AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 2 and 12 and amend claims 1, 3, 11 and 13 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

one or more further circuits responsive to said performance control signal to operate so as to support said desired data processing performance level of said processor; wherein

at least while responding to a change in said performance control signal, said one or more further circuits are operable to generate a current operation signal indicative of current operation of said one or more further circuits, wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels, said current operation signal being indicative of a maximum power supply voltage that can currently be supported by said voltage controller.

2. (cancelled).

3. (currently amended) Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock

frequency, said ~~currently~~current operation signal being indicative of a clock frequency that is currently being generated by said clock generator.

4. (original) Apparatus as claimed in claim 3, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

5. (original) Apparatus as claimed in claim 4, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

6. (original) Apparatus as claimed in claim 2, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

7. (original) Apparatus as claimed in claim 1, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

8. (original) Apparatus as claimed in claim 7, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

9. (original) Apparatus as claimed in claim 8, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when a power signal is generated with a voltage level sufficient to support said intermediate clock signal frequency.

10. (original) Apparatus as claimed in claim 7, wherein a priority signal serves to trigger said one or more further circuits change to support a maximum data processing performance level independently of said performance control signal.

11. (currently amended) A method of processing data, said method comprising the steps of:

performing data processing operations with a processor, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

in response to said performance control signal, operating one or more further circuits so as to support said desired data processing performance level of said processor; wherein

at least while responding to a change in said performance control signal, said one or more further circuits are operable to generate a current operation signal indicative of current operation of said one or more further circuit, wherein said one or more further circuit include a voltage

controller operable to generate a power signal for said processor at a plurality of different voltage levels, said current operation signal being indicative of a maximum power supply voltage that can currently be supported by said voltage controller.

12. (cancelled).

13. (currently amended) A method as claimed in claim 11, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said ~~currently~~current operation signal being indicative of a clock frequency that is currently being generated by said clock generator.

14. (original) A method as claimed in claim 13, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

15. (original) A method as claimed in claim 14, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

16. (original) A method as claimed in claim 12, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency

when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

17. (original) A method as claimed in claim 12, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said further circuit is operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

18. (original) A method as claimed in claim 17, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

19. (original) A method as claimed in claim 18, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when a power signal is generated with a voltage level sufficient to support said intermediate clock signal frequency.

20. (original) A method as claimed in claim 17, wherein a priority signal serves to trigger said further circuit change to support a maximum data processing performance level independently of said performance control signal.